REMARKS

The 1 June 2005 official action addressed claims 14 and 16-32. Claims 14, 16, 21, 25, 27 and 31 are amended. Claim 20 is canceled.

Overview of amendments

Independent claim 14 is amended to specify that the SOI substrate is formed by placing layers of two separate substrates in contact and applying heat to bond the layers.

Independent claims 14, 21 and 27 are also amended to specify that a silicon carbide thermal dissipation layer provides dissipation of heat from the substrate, such as from a FinFET or MOSFET formed on the substrate.

Response to rejections

Claims 14-18 were rejected as being anticipated by Felker (U.S. 6,508,948). Claim 19 was rejected as being obvious over Felker. Claim 20 was were indicated to be obvious over Felker in view of Maa (U.S. 6,562,703). Claims 21-26 were rejected as being obvious over Hu (U.S. 6,413,802) in view of Felker. Claims 27-32 were rejected as being obvious over Felker in view of White (U.S. 6,130,102).

All of the claims as now amended are distinguished over the cited references in that none of the cited references teaches the use of a thermal dissipation layer in an SOI substrate beneath a dielectric layer of the SOI substrate to dissipate heat from a semiconductor layer and dielectric layer of the substrate or from a FinFET or MOSFET formed on the substrate. Therefore all claims are allowable on this basis.

Claims 14 and 16-19 as now amended are further distinguished over the cited references in that none of the cited references teaches the formation of an SOI substrate by a process wherein a dielectric layer of a first substrate is placed in contact with a silicon carbide layer of a second substrate and then heated to bond

the dielectric layer to the silicon carbide layer. Therefore claims 14 and 16-19 are allowable on this additional basis.

Claims 27-32 as now amended are further distinguished over the combination of Felker and White in that the cited references do not teach providing a SOI substrate comprising a semiconductor layer, a dielectric layer and a silicon carbide layer, and then performing processing that forms trenches in the semiconductor layer and forms a MOSFET in an active area defined by the trenches. White is cited as teaching such a substrate, however the portions of White that are cited as corresponding to the claimed semiconductor layer, dielectric layer and silicon carbide layer are, respectively, White's gate dielectric 18, gate electrode 20 and interlevel dielectric 22. These cannot constitute the substrate layers required by the present claims, since the present claims require these layers to be provided, then require etching to occur to form an active region, and then require formation of a MOSFET in the active region. Once the cited portions of White are provided, they are not etched further to form an active region and then form a MOSFET. Therefore claims 27-32 are allowable on this additional basis.

The foregoing amendments and remarks address all bases for objection and rejection and are believed to place the case in condition for allowance. The examiner is invited to contact the undersigned to resolve any remaining issues.

Respectfully submitted,

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FOLEY & LARDNER LLP
Customer Number 23392
Telephone 310 975 7964
Fax 310 557 8475

Ronald Coslick
Attorney for Applicant
Registration No. 36,489